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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,714	12/20/2000	Mohamed S. El-Hennawey	91436-283CIP	3264

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EXAMINER	
ALI, SYED J	

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,714	EL-HENNAWEY ET AL.	
	Examiner	Art Unit	
	Syed J Ali	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are pending in this application.

Claim Objections

2. Claims 1, 4, 6, and 9-11 are objected to because of the following informalities:

In claims 1, 4, 6, and 9-11, "optimised" should read "optimized" in all cases.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leondires et al. (USPN 5,841,763) (hereinafter Leondires) in view of Crawford (USPN 4,709.344) in view of Fadavi-Ardekani et al. (USPN 6,401,176) (hereinafter Fadavi).

As per claim 1, Leondires teaches the invention as claimed, including a method of processing communication channels, comprising:

for each of a plurality of channels:

undertaking a given channel processing task for a given channel with one processor of a plurality of processors, said one processor optimized for said given channel processing task (col. 3 line 44 - col. 4 line 5, "The host processor can use the status information to determine which digital signal processor is to be assigned to perform the processing required by a particular function").

Crawford teaches the invention as claimed, including the following limitations not shown by Leondires, specifically when said given channel processing task for said given channel changes to a new channel processing task for which said one processor is not optimized,

moving processing of said given channel to a different one of said plurality of processors, said different one of said processors being optimized for said new channel processing task (col. 7 lines 36-48, "The input signals to the correspondence control can be sourced from within the post-processor 34, allowing automatic control and reassignment capabilities").

Fadavi teaches the invention as claimed, including the following limitations not shown by Leondires or Crawford, specifically:

storing instance data for said given channel processing task in a memory which may be associated with any one of said plurality of processors such that said instance data is associated with said one processor (col. 4 lines 1-16, "The switching circuitry in the shared synchronous memory 200*a* allows access to a common memory block by a selected one of the plurality of agents 100 to 108 at any one time"); and

when said given channel processing task for said given channel changes to a new channel processing task for which said one processor is not optimized,

changing association of said stored given channel instance data to an association with said different processor (col. 4 lines 24-35, "a selection signal is transmitted by the arbiter 102*a* to the switching elements, e.g., multiplexing elements in the shared synchronous memory 200*a* on a corresponding selection signal path").

It would have been obvious to one of ordinary skill in the art to combine Leondires, Crawford, and Fadavi since the system disclosed by Leondires fails to adaptively assign signals to be processed among a plurality of processors. Rather, an initial determination is made for what processor is best suited to process the signal, and that processor is assigned to process the signal. Furthermore, the memory used to store data used to process a task is local to the particular processor, further limiting the dynamic reassignment capabilities. Crawford provides the improvement of multiplexing the input signals to the processors, thereby controlling what processor processes a signal based on the type of signal, and is dynamically adjustable utilizing a post-processor. However, neither Leondires nor Crawford teaches of a global memory for storing instance data used to process a signal. Rather, each processor is configured for a particular function, and the functionality is pre-programmed for the processor, or downloaded to the processor's specific memory. Fadavi provides a global memory that is shared by all processors in the system. This allows a great deal of flexibility in assigning tasks to a processor, as the processor itself would not require reconfiguration. Rather, the multiplexer simply needs to change the select signal such that any processor can use the shared memory for the data needed to process the signal.

As per claim 4, Leondires teaches the invention as claimed, including the method of claim 1 wherein said moving comprises consulting a table for a processor optimized to said new channel processing task (col. 18 lines 19-36, "To facilitate the process of identifying available DSPs, the host 174 tracks information, by way of status tables in memory 175, such as...which DSPs are assigned to perform each of the functions of Table 2, and the number of available channels on each DSP that is assigned to a particular function").

As per claim 5, Fadavi teaches the invention as claimed, including the method of claim 1 wherein said memory is a multiplexed memory (col. 4 lines 49-58, "Activation of any one of the select lines 110 to 113 steers the appropriate circuitry corresponding to the clock, address, data, and control multiplexers in the shared synchronous memory 200*a* toward the winning agent").

As per claim 6, Leondires teaches the invention as claimed, including the method of claim further comprising, where said one processor is optimized for said new channel processing task, undertaking said new channel processing task for said given channel at said one processor (col. 3 line 44 - col. 4 line 5, "the host processor, upon recognizing that processing for a particular function is required, can examine the stored status information to determine if there is any digital signal processor, which is already configured to perform the required processing for the particular function and which can accommodate an additional communication connection").

As per claim 7, Leondires teaches the invention as claimed, including the method of claim 6 further comprising keeping a table with an identification of available ones of said

plurality of processors and an identification of processing tasks handled by said available ones of said plurality of processors (col. 18 lines 19-36, "To facilitate the process of identifying available DSPs, the host 174 tracks information, by way of status tables in memory 175, such as...which DSPs are assigned to perform each of the functions of Table 2, and the number of available channels on each DSP that is assigned to a particular function").

As per claim 8, Fadavi teaches the invention as claimed, including the method of claim 5 wherein said changing association comprises overwriting a latch holding an address of said one processor with an address of said different processor (col. 4 lines 1-16, "the shared synchronous memory 200*a* in Fig. 2 includes appropriate switching circuitry including latches and multiplexers associated with each agent 100 to 108").

As per claim 9, Leondires teaches the invention as claimed, including a method of processing communication channels comprising:

at each of a plurality of processors:

undertaking a channel processing task (col. 3 line 44 - col. 4 line 5, "the host processor assigns that processor to perform the processing for the particular function"); and

when said channel processing task changes to a new channel processing task:

referencing a table to identify a processor of said plurality of processors optimized to said new channel processing task (col. 3 line 44 - col. 4 line 5, "The host processor can use the status information to determine which digital signal

processor is to be assigned to perform the processing required by a particular function").

Crawford teaches the invention as claimed, including the following limitations not shown by Leondires, specifically:

prompting said new task optimized processor to assume processing of said channel (col. 7 lines 36-48, "The input signals to the correspondence control can be sourced from within the post-processor 34, allowing automatic control and reassignment capabilities").

Fadavi teaches the invention as claimed, including the following limitations not shown by Leondires or Crawford, specifically:

using a multiplexed memory for channel instance memory (col. 4 lines 49-58, "Activation of any one of the select lines 110 to 113 steers the appropriate circuitry corresponding to the clock, address, data, and control multiplexers in the shared synchronous memory 200*a* toward the winning agent"), and

arranging for an associator to associate instance memory for said channel with said new task optimized processor (col. 4 lines 24-35, "a selection signal is transmitted by the arbiter 102*a* to the switching elements, e.g., multiplexing elements in the shared synchronous memory 200*a* on a corresponding selection signal path").

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leondires in view of Crawford in view of Fadavi in view of Weiss et al. (USPN 5,526,363) (hereinafter Weiss).

As per claim 2, Weiss teaches the invention as claimed, including the following limitations not shown by the combination of Leondires, Crawford, and Fadavi, specifically the method of claim 1 wherein said given channel instance data comprises a history buffer storing historical data samples for a signal on said given channel (col. 3 lines 30-58, "A memory 18 in accordance with the invention having a shared hash table is shown in Fig. 2A. This memory has a separate history buffer 20A-20D for each of four channels to which the node 12 is transmitting").

It would have been obvious to one of ordinary skill in the art to combine Leondires, Crawford, and Fadavi for reasons discussed above in reference to claim 1. Further, it would have been obvious to one of ordinary skill in the art to add Weiss to the combination thereof since it would allow predictive assignment of processing channels to processors, thereby increasing the efficiency of the system by utilizing a processor that is best suited to process a particular signal..

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leondires in view of Crawford in view of Fadavi in view of Lin et al. (USPN 6,606,306) (hereinafter Lin).

As per claim 3, Lin teaches the invention as claimed, including the following limitations not shown by the combination of Leondires, Crawford, and Fadavi, specifically the method of claim 1 wherein said given channel instance data comprises a jitter buffer (col. 3 line 66 - col. 4 line 19, "Processing module 22 may receive from SRM module 14 initiation information

indicating a number of participants in the media conference and, in response, create in memory 24 one or more jitter buffers 26*a*, 26*b*, and 26*c* [collectively, buffers 26] for each participant").

It would have been obvious to one of ordinary skill in the art to combine Leondires, Crawford, and Fadavi for reasons discussed above in reference to claim 1. Further, it would have been obvious to one of ordinary skill in the art to add Lin to the combination thereof since Leondires is also directed to a conferencing system, and the use of a jitter buffer would enable smoother processing of audio and visual signals, thereby improving the quality of the signal processing.

7. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leondires in view of Fadavi.

As per claim 10, Leondires teaches the invention as claimed, including a multiprocessor system for processing communications channels, comprising:

a plurality of processors, each optimized for at least one channel processing task and each having processor memory for storing information associating different channel processing tasks to different ones of said processors (col. 3 line 44 - col. 4 line 5, "the host processor assigns that processor to perform the processing for the particular function"; col. 9 lines 50-64, "All DSPs, on both the parent and child boards, are identically equipped with...memory storage").

Fadavi teaches the invention as claimed, including the following limitations not shown by Leondires, specifically:

a multiplexed memory for storing channel processing instance data for each of said plurality of processors (col. 4 lines 49-58, "Activation of any one of the select lines 110 to 113 steers the appropriate circuitry corresponding to the clock, address, data, and control multiplexers in the shared synchronous memory 200*a* toward the winning agent");

an associator for associating channel processing instance data for each channel with one of said plurality of processors (col. 4 lines 24-35, "a selection signal is transmitted by the arbiter 102*a* to the switching elements, e.g., multiplexing elements in the shared synchronous memory 200*a* on a corresponding selection signal path"); and

each processor of said plurality of processors operable to, on a channel processing task for a channel currently being processed by said each processor changing to a new task,

arrange for said associator to associate instance data for said channel with a processor optimized to said new task (col. 4 lines 24-35, "a selection signal is transmitted by the arbiter 102*a* to the switching elements, e.g., multiplexing elements in the shared synchronous memory 200*a* on a corresponding selection signal path", wherein the select signal indicates what processor is associated with the memory).

As per claim 11, Leondires teaches the invention as claimed, including the system of claim 10 further comprising a host for, on a channel processing task for a channel currently being processed by a given processor changing to a new task, sending to said given processor an indication of said processor optimized to said new task (col. 7 lines 36-48, "The input signals to the correspondence control can be sourced from within the post-processor 34, allowing

automatic control and reassignment capabilities", wherein the correspondence control acts as the host that controls the distribution of input signals).

As per claim 12, Fadavi teaches the invention as claimed, including the system of claim 10 wherein said associator comprises a latch for channel instance data of a given channel, each said latch being latched to a given processor processing said given channel and arranged such that only said given processor may change said latch to a new processor (col. 4 lines 1-16, "the shared synchronous memory 200*a* in Fig. 2 includes appropriate switching circuitry including latches and multiplexers associated with each agent 100 to 108").

As per claim 13, Fadavi teaches the invention as claimed, including the system of claim 12 wherein said associator further comprises a multiplexer mapping memory read/write requests from said given processor to instance channel data for said given channel in said shared memory (col. 4 lines 49-58, "Activation of any one of the select lines 110 to 113 steers the appropriate circuitry corresponding to the clock, address, data, and control multiplexers in the shared synchronous memory 200*a* toward the winning agent").

As per claim 14, Leondires teaches the invention as claimed, including the system of claim 13 wherein each of said plurality of processors is a digital signal processor ["DSP"] (col. 4 lines 60-67, "the invention is directed to methods and apparatus for distributing the processing requirements of an audio-video conferencing system between a plurality of digital signal processors").

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

USPN 6,038,400 to Bell et al. teaches interface circuitry that adapts to a changing signal.

USPN 6,108,343 to Cruickshank et al. is mentioned by Applicant in the specification, and teaches a reconfigurable DSP with a local memory storing channel instance data.

USPN 6,526,068 to Smith teaches a reconfigurable shared memory for a single DSP.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
March 2, 2004

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